



**MIPS® 4K™/5K™ LV (FPGA Module)  
Specification Update**

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|       |                                                                             |    |
|-------|-----------------------------------------------------------------------------|----|
| 1     | Preface .....                                                               | 4  |
| 1.1   | Emphasis of Range Violations and Document Modifications .....               | 4  |
| 2     | Specification Updates to 4K/5K class cores implemented on FPGA Module ..... | 5  |
| 2.1   | Basic Information .....                                                     | 5  |
| 2.2   | Errata Information .....                                                    | 6  |
| 2.3   | Supply Voltages and Environmental Conditions .....                          | 7  |
| 2.4   | Test-related Pin-out .....                                                  | 7  |
| 2.5   | DC Specifications .....                                                     | 7  |
| 2.6   | AC Specifications .....                                                     | 8  |
| 2.6.1 | Clock Signals .....                                                         | 8  |
| 2.6.2 | Other functional pins .....                                                 | 8  |
| 2.7   | PLL Connections and Loop Filter .....                                       | 12 |
| 3     | LV Errata .....                                                             | 13 |
| 4     | References .....                                                            | 15 |
| 5     | Revision history .....                                                      | 16 |

# 1 Preface

This document communicates updates to the specifications of the family of MIPS32™ 4K™ and MIPS64™ 5K™ Processor Lead Vehicles contained in the document *MIPS 4K/5K™ Lead Vehicle Datasheet*, [Ref \[1\]](#).

There are variations in the characteristics of the Lead Vehicles. These are due to the variations in the type, revision, and configuration of the Lead Vehicle, and they are dependent on the vendor, the process technology, and the production series. Through the on-going validation and characterization of the Lead Vehicles, MIPS identifies updates and additions to the information in the documentation for the Lead Vehicles. The Specification Updates in this document are specific to the

- *MIPS32 4K Processor Lead Vehicles implemented in the FPGA Module (FPGA 1600)*
- *MIPS64 5K Processor Lead Vehicles implemented in the FPGA Module (FPGA 3200/2600)*

The Specification Updates can be classified as deviations from the generic specifications, additional information, or defects. This document covers any 4K or 5K class core (4K, 4KE, 4KS, 5K) implemented on the FPGA Module, and not just one particular implementation. Where there is a difference between the implementations, these are identified by the official name of the bitfile used to program the FPGA on the FPGA Module.

The document is primarily intended for hardware system developers using the FPGA Module implementation of a MIPS32 4K or MIPS64 5K class core to prototype a SOC, using e.g. the SEAD-2 platform from MIPS.

The document presents additional information and detailed descriptions of deviations from the specifications in the datasheet. There are sections for updates to the chip pin description, AC & DC specifications, power supply, operating frequency, and other specification updates. Note: Since this document covers a FPGA Module rather than a silicon LV implementation, some aspects will differ from the traditional specification update documents.

All 4K/5K LV's provide the ability of the software to configure certain aspects of the physical hardware configuration, most notably the cache configuration can be "downgraded" under software control to experiment with the performance effects. This configuration ability is described in [Ref \[6\]](#).

Defects are listed in overview form in the errata information section. A detailed description of the defects are given in [Section 3, "LV Errata"](#). This includes description of the problem, the implication on the system, a suggested work around, and status. The status of an errata will be described by one of the following codes:

**Table 1 Status Codes Used In Summary Tables**

| Code  | Description                                                              |
|-------|--------------------------------------------------------------------------|
| Open  | This issue is under investigation.                                       |
| Fix   | This issue is intended to be fixed in a future version of the component. |
| Fixed | This issue has been fixed in a previous version.                         |
| NoFix | There are no plans to fix this issue.                                    |
| Doc   | The appropriate documents will be updated in the future.                 |

## 1.1 Emphasis of Range Violations and Document Modifications

Throughout the document a shaded field in a table is used to emphasize that this value is deviating from, or violating, the range specified in the datasheet.

## 2 Specification Updates to 4K/5K class cores implemented on FPGA Module

In this section specific information on this particular Lead Vehicle is provided. The information is structured as a set of sub-sections containing specifications that must be present for each Lead Vehicle. These sub-sections are a supplement to the datasheet and consist of

- Basic Information
- Errata Information
- Supply Voltages and Environmental Conditions
- Test-related Pin-out
- DC Specifications
- AC Specifications
- PLL Connections and Loop Filter

The remaining sections contains Specification Updates that are unique for this Lead Vehicle and thus not covered elsewhere.

### 2.1 Basic Information

The basic information for the Lead Vehicle is summarized in [Table 2](#) (4K cores) and [Table 3](#) (5K cores). All the 4K core FPGA implementations are intended for use on the FPGA Module (FPGA 1600), whereas the 5K implementations must be used with FPGA Module (FPGA 3200/2600). It is not possible to use a bitfile for a specific LV implementation on a different FPGA Module than it was built for.

**Table 2 Lead Vehicle Information (4K cores)**

| IPDP number and revision | Type | Data Cache                                | Instr. Cache                              | MMU                       | EJTAG support                                          | RTL version | Static inputs<br>EJ_ManufID[11:0],<br>EJ_PartNumber[15:0],<br>EJ_Version[3:0] | CP0 PRID Value |
|--------------------------|------|-------------------------------------------|-------------------------------------------|---------------------------|--------------------------------------------------------|-------------|-------------------------------------------------------------------------------|----------------|
| IPDP00102 rev.01.00      | 4KEc | 4-way,<br>4 KB<br>sets:<br>16 KB<br>total | 4-way,<br>4 KB<br>sets:<br>16 KB<br>total | TLB<br>16 dual<br>entries | Version 2.6<br>4 I breaks,<br>2 D breaks<br>Trace: no  | 2.00        | 0x127, 0x0700, 0                                                              | 0x018440       |
| IPDP00131 rev.01.00      | 4KSc | 4-way,<br>4 KB<br>sets:<br>16 KB<br>total | 4-way,<br>4 KB<br>sets:<br>16 KB<br>total | TLB<br>16 dual<br>entries | Version 2.6<br>4 I breaks,<br>2 D breaks<br>Trace: no  | 2.00        | 0x127, 0x0900, 0                                                              | 0x018640       |
| IPDP00128 rev.01.00      | 4KEp | 4-way,<br>4 KB<br>sets:<br>16 KB<br>total | 4-way,<br>4 KB<br>sets:<br>16 KB<br>total | Fixed                     | Version 2.6<br>4 I breaks,<br>2 D breaks<br>Trace: yes | 2.00F37     | 0x127, 0x0700, 0                                                              | 0x018540       |

**Table 2 Lead Vehicle Information (4K cores)**

| IPDP number and revision | Type | Data Cache                          | Instr. Cache                        | MMU                    | EJTAG support                                          | RTL version | Static inputs<br>EJ_ManuffID[11:0],<br>EJ_PartNumber[15:0],<br>EJ_Version[3:0] | CP0 PRID Value |
|--------------------------|------|-------------------------------------|-------------------------------------|------------------------|--------------------------------------------------------|-------------|--------------------------------------------------------------------------------|----------------|
| IPDP00102 rev. 01.01     | 4KEc | 4-way,<br>4 KB sets:<br>16 KB total | 4-way,<br>4 KB sets:<br>16 KB total | TLB<br>16 dual entries | Version 2.6<br>4 I breaks,<br>2 D breaks<br>Trace: yes | 2.2.0       | 0x127, 0x0700, 0                                                               | 0x018448       |
| IPDP00132 rev.01.00      | 4KEm | 4-way,<br>4 KB sets:<br>16 KB total | 4-way,<br>4 KB sets:<br>16 KB total | Fixed                  | Version 2.6<br>4 I breaks,<br>2 D breaks<br>Trace: yes | 2.2.0       | 0x127, 0x0700, 0                                                               | 0x018548       |
| IPDP00128 rev.01.01      | 4KEp | 4-way,<br>4 KB sets:<br>16 KB total | 4-way,<br>4 KB sets:<br>16 KB total | Fixed                  | Version 2.6<br>4 I breaks,<br>2 D breaks<br>Trace: yes | 2.2.0       | 0x127, 0x0700, 0                                                               | 0x018548       |
| IPDP00131 rev.01.01      | 4KSc | 4-way,<br>4 KB sets:<br>16 KB total | 4-way,<br>4 KB sets:<br>16 KB total | TLB<br>16 dual entries | Version 2.6<br>4 I breaks,<br>2 D breaks<br>Trace: yes | 2.2.0       | 0x127, 0x0900, 0                                                               | 0x018648       |

**Table 3 Lead Vehicle Information (5K cores)**

| IPDP number and revision | Type | Data Cache                          | Instr. Cache                        | MMU                    | EJTAG support                                         | RTL version | Static inputs<br>EJ_ManuffID[11:0],<br>EJ_PartNumber[15:0],<br>EJ_Version[3:0] | CP0 PRID Value |
|--------------------------|------|-------------------------------------|-------------------------------------|------------------------|-------------------------------------------------------|-------------|--------------------------------------------------------------------------------|----------------|
| IPDP00130 rev.01.00      | 5Kf  | 4-way,<br>8 KB sets:<br>32 KB total | 4-way,<br>8 KB sets:<br>32 KB total | TLB<br>48 dual entries | Version 2.6<br>4 I breaks,<br>2 D breaks<br>Trace: no | 2.3B.3      | 0x127, 0x0320, 0                                                               | 0x01810A       |

## 2.2 Errata Information

Table 4 contains an overview of the present errata information on these FPGA LV implementations of the MIPS 4K/5K class cores. The listed errata information only concerns the FPGA LV implementations and not the MIPS 4K/5K class core itself. For errata information on the latter, see [Ref \[2\]](#), [Ref \[3\]](#), [Ref \[4\]](#) (MIPS 4K cores) or [Ref \[5\]](#) (MIPS 5K cores).. [Section 3, "LV Errata"](#) contains a detailed description of the FPGA LV errata.

**Table 4 Errata information**

| Errata# | Description                       |
|---------|-----------------------------------|
| L1      | SysAD operation is not supported. |
| L2      | PLL operation is not supported.   |

**Table 4 Errata information**

| Errata# | Description                     |
|---------|---------------------------------|
| L3      | GCLKB output is not functional. |

### 2.3 Supply Voltages and Environmental Conditions

This is N/A as the FPGA Module receives the power supply from the base board.

### 2.4 Test-related Pin-out

This is N/A as the FPGA Module does not implement the test-pins of the silicon LVs.

### 2.5 DC Specifications

The I/O cells on this Lead Vehicle are from the Xilinx Virtex-E cell library.

**Table 5 Recommended Operating Condition**

| Parameter       | Description               | Min   | Nom   | Max   |
|-----------------|---------------------------|-------|-------|-------|
| VDD             | I/O buffer supply voltage | 3.0 V | 3.3 V | 3.6 V |
| V <sub>I</sub>  | Input voltage             | 0 V   |       | VDD   |
| V <sub>O</sub>  | Output voltage            | 0 V   |       | VDD   |
| V <sub>IH</sub> | High-level input voltage  | 2.0 V |       | VDD   |
| V <sub>IL</sub> | Low-level input voltage   | 0 V   |       | 0.8 V |

**Table 6 Electrical Characteristics**

| Parameter       | Condition                           | Min  | Max            |
|-----------------|-------------------------------------|------|----------------|
| V <sub>OH</sub> | I <sub>O</sub> = rated              | 2.4V |                |
| V <sub>OL</sub> | I <sub>O</sub> = rated              |      | 0.4V           |
| I <sub>IH</sub> | V <sub>I</sub> = V <sub>I</sub> max |      | +/- 10 $\mu$ A |
| I <sub>IL</sub> | V <sub>I</sub> = V <sub>I</sub> max |      | +/- 10 $\mu$ A |
| I <sub>OZ</sub> | VDD = nominal V                     |      | +/- 10 $\mu$ A |

The input and output drivers are all of the same type, LVTTTL\_S12. [Table 7](#) lists the capacitive loading at the package pin for all used IO driver types. For the output drivers the rated I<sub>O</sub> is included, as well. The capacitive loading (i.e. the capacitance on the input pins of the input drivers, and the capacitance on the output of the output driver) are the typical values for a nominal process under nominal conditions at VDD = 3.3 V.

**Table 7 Driver Characteristics**

| Driver     | I/O | Load Factor | I <sub>O</sub> |
|------------|-----|-------------|----------------|
| LVTTTL_S12 | I/O | <8 pF       | 12mA           |

## 2.6 AC Specifications

This section shows any deviations of the AC specifications from the corresponding descriptions in the Datasheet. First, an overview of the clock AC specifications is provided. Then, tables for the AC requirements of the pins are presented.

### 2.6.1 Clock Signals

Table 8 shows the frequency and duty cycle ranges for all the input clock pins in the Lead Vehicle. The duty cycle is here specified as the percentage of the cycle where the phase is high.

**Table 8 Clocking Frequency and Duty Cycle Range**

| Pin, Mode                                                            | Min                           | Max                 |
|----------------------------------------------------------------------|-------------------------------|---------------------|
| Core clock frequency range                                           | 0 MHz                         | 15 MHz              |
| GCLK frequency range, SysAD64 (PLL enabled), x2 mode => GMULT[1:0]=1 | SysAD operation not supported |                     |
| GCLK frequency range, SysAD64 (PLL enabled), x3 mode => GMULT[1:0]=2 |                               |                     |
| GCLK frequency range, SysAD64 (PLL enabled), x4 mode => GMULT[1:0]=3 |                               |                     |
| GCLK duty cycle, SysAD64 (PLL enabled)                               |                               |                     |
| GCLK frequency range, core bond-out (PLL disabled)                   | 0 MHz                         | 15 MHz              |
| GCLK duty cycle, core bond-out (PLL disabled)                        | 40                            | 60                  |
| ETCK frequency range                                                 | 0 MHz                         | 10 MHz <sup>a</sup> |
| ETCK duty cycle                                                      | 40                            | 60                  |

a. Due to ETDO timing.

### 2.6.2 Other functional pins

The following three tables lists the AC/DC pin specifications.

**Table 9 AC/DC Pin Specifications For Shared Function Pins**

| Pin name   | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|------------|------|-------------|--------------------|-----------------|------------------|------------------|------------------|-----------------|
| GCLK       | I    | LVTTL_S12   |                    | -               |                  |                  |                  |                 |
| GCLKB      | O    | LVTTL_S12   |                    | DC              |                  |                  |                  |                 |
| GRST2_N    | I    | LVTTL_S12   |                    | DC              |                  |                  |                  |                 |
| GBYPASS    | I    | LVTTL_S12   |                    | DC              |                  |                  |                  |                 |
| GMULT[1:0] | I    | LVTTL_S12   |                    | DC              |                  |                  |                  |                 |
|            |      |             |                    |                 |                  |                  |                  |                 |
| CBIGEN     | I    | LVTTL_S12   |                    | DC              |                  |                  |                  |                 |



Table 9 AC/DC Pin Specifications For Shared Function Pins

| Pin name     | Type   | Buffer Type | External load [pF] | Reference Clock     | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|--------------|--------|-------------|--------------------|---------------------|------------------|------------------|------------------|-----------------|
| CTIMER5      | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| CSYSAD       | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| CPIPEWR      | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| C4WBLK       | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| ETCK         | I      | LVTTL_S12   |                    | -                   |                  |                  |                  |                 |
| ETMS         | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| ETDI         | I      | LVTTL_S12   |                    | ETCK                |                  |                  | 15               | 0               |
| ETDO         | O (3S) | LVTTL_S12   | 25                 | ETCK <sup>a</sup>   | 2                | 30               |                  |                 |
| ETRST_N      | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| EDINT        | I      | LVTTL_S12   |                    | ASYNC               |                  |                  |                  |                 |
| ERES[1:0]    | O      | LVTTL_S12   |                    |                     |                  |                  |                  |                 |
| TR_Probe_n   | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| TR_TrigIn    | I      | LVTTL_S12   |                    | ASYNC               |                  |                  |                  |                 |
| TR_TrigOut   | O      | LVTTL_S12   | 25                 | ASYNC               |                  |                  |                  |                 |
| TR_Clk       | O      | LVTTL_S12   | 25                 |                     |                  |                  |                  |                 |
| TR_Data[7:0] | O      | LVTTL_S12   | 25                 | TR_Clk <sup>b</sup> | -3               | 3                |                  |                 |
| TR_DM        | O      | LVTTL_S12   | 25                 | ASYNC               |                  |                  |                  |                 |
| TSE          | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| TSM          | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| TSI          | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| TSO          | O      | LVTTL_S12   | 25                 |                     |                  |                  |                  |                 |
| TIN[3:0]     | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| TIN_N[3:0]   | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| TOUT[3:0]    | O      | LVTTL_S12   |                    |                     |                  |                  |                  |                 |
| MBUS[1:0]    | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| MINP[2:0]    | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |
| MINP_N[2:0]  | I      | LVTTL_S12   |                    | DC                  |                  |                  |                  |                 |

- a. The ETDO output timing is specified relative to the negative edge of ETCK.
- b. The TR\_Data is DDR data output with regards to TR\_Clk. See the relevant PDtrace specification for details. The timing specification is the maximum jitter of the TR\_Data output edges wrt. the TR\_Clk edges (both positive and the “ideally” placed negative edge).

**Table 10 AC/DC pin specs for SysAD64 mode**

| Pin name     | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|--------------|------|-------------|--------------------|-----------------|------------------|------------------|------------------|-----------------|
| GRST_N       | I    | LVTTL_S12   |                    | ASYNC           |                  |                  |                  |                 |
| SSYSAD[63:0] | I/O  | LVTTL_S12   | 25                 | GCLK            |                  |                  |                  |                 |
| SSYSCMD[8:0] | I/O  | LVTTL_S12   | 25                 | GCLK            |                  |                  |                  |                 |
| SSYSADC[7:0] | I/O  | LVTTL_S12   | 25                 | GCLK            |                  |                  |                  |                 |
| SSYSCMDP     | I/O  | LVTTL_S12   | 25                 | GCLK            |                  |                  |                  |                 |
| SRDRDY_N     | I    | LVTTL_S12   |                    | GCLK            |                  |                  |                  |                 |
| SWRRDY_N     | I    | LVTTL_S12   |                    | GCLK            |                  |                  |                  |                 |
| SVALIDIN_N   | I    | LVTTL_S12   |                    | GCLK            |                  |                  |                  |                 |
| SVALIDOUT_N  | O    | LVTTL_S12   | 25                 | GCLK            |                  |                  |                  |                 |
| SEXTRQST_N   | I    | LVTTL_S12   |                    | GCLK            |                  |                  |                  |                 |
| SRELEASE_N   | O    | LVTTL_S12   | 25                 | GCLK            |                  |                  |                  |                 |
|              |      |             |                    |                 |                  |                  |                  |                 |
| IINT_N[5:0]  | I    | LVTTL_S12   |                    | ASYNC           |                  |                  |                  |                 |
| INML_N       | I    | LVTTL_S12   |                    | ASYNC           |                  |                  |                  |                 |

SysAD operation not supported.

**Table 11 AC/DC pin specs for core bond-out mode**

| Pin name       | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|----------------|------|-------------|--------------------|-----------------|------------------|------------------|------------------|-----------------|
| EB_A[35:2]     | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_WData[63:0] | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_RData[63:0] | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| EB_BE[7:0]     | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_AValid      | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_Write       | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_Instr       | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_Burst       | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_BFirst      | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |

Table 11 AC/DC pin specs for core bond-out mode (Continued)

| Pin name          | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|-------------------|------|-------------|--------------------|-----------------|------------------|------------------|------------------|-----------------|
| EB_BLast          | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_BLen[1:0]      | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_ARdy           | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| EB_RdVal          | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| EB_WDRdy          | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| EB_RBErr          | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| EB_WBErr          | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| EB_WWBE           | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EB_EWBE           | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| EB_SBlock         | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
|                   |      |             |                    |                 |                  |                  |                  |                 |
| SI_Int[5:0]       | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| SI_NMI            | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| SI_ColdReset      | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| SI_Reset          | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| SI_MergeMode[1]   | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| SI_SimpleBE[0]    | I    | LVTTL_S12   |                    | GCLK            |                  |                  | 6                | 0               |
| SI_RP             | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| SI_Sleep          | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| SI_TimerInt       | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| SI_ERL            | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| SI_EXL            | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
|                   |      |             |                    |                 |                  |                  |                  |                 |
| EJ_PerRst         | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EJ_PrRst          | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EJ_SRstE          | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| EJ_DebugM (TR_DM) | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
|                   |      |             |                    |                 |                  |                  |                  |                 |
| PM_DCacheHit      | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_DCacheMiss     | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_ICacheHit      | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |

**Table 11 AC/DC pin specs for core bond-out mode (Continued)**

| Pin name          | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|-------------------|------|-------------|--------------------|-----------------|------------------|------------------|------------------|-----------------|
| PM_ICacheMiss     | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_InstrnComplete | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_ITLBHit        | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_ITLBMiss       | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_JTLBHit        | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_JTLBMiss       | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_WTBMerge       | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_WTBNoMerge     | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_DTLBHit        | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |
| PM_DTLBMiss       | O    | LVTTL_S12   | 25                 | GCLK            | 3                | 10               |                  |                 |

## 2.7 PLL Connections and Loop Filter

This section is not applicable, as the FPGA Module does not implement the PLL present in the silicon LVs. Only the PLL bypass mode is supported.

### 3 LV Errata

#### ***L1. SysAD operation is not supported***

Problem:

The SysAD functionality in this LV implementation does not work. The device will operate in bond-out mode regardless of the value on the CSYSAD input pin.

Implication:

None, really. The FPGA Module is currently only intended to be used on SEAD/SEAD-2 platforms, which only use the bond-out operation mode anyway.

Work around:

None.

Status:

NoFix.

#### ***L2. PLL operation is not supported***

Problem:

The PLL functionality specified in the LV Datasheet is not implemented. The device will operate in PLL bypass mode regardless of the value on the GBYPASS input pin.

Implication:

Similar to L1 - none. As SEAD/SEAD-2 does not attempt to use the device in PLL mode, this is not a real limitation for the intended use.

Work around:

None.

Status:

NoFix.

#### ***L3. GCLKB output is not functional***

Problem:

The GCLKB output is not driven with the correct value. Since GCLKB is present for debug purposes anyway, this should be irrelevant.

Implication:

None.

Work around:

None.

Status:

NoFix.

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## 4 References

- [1] MIPS 4K/5K™ Lead Vehicle Datasheet  
Document no: MD00001  
MIPS Technologies, Inc.
- [2] MIPS32 4K™ Processor Core Family RTL Errata Sheet  
Document no: MD00003  
MIPS Technologies, Inc.
- [3] MIPS32 4KE™ Processor Core Family RTL Errata Sheet  
Document no: MD00110  
MIPS Technologies, Inc.
- [4] MIPS32 4KSc™ Processor Core RTL Errata Sheet  
Document no: MD00133  
MIPS Technologies, Inc.
- [5] MIPS64 5K™ Processor Core Family RTL Errata Sheet  
Document no: MD00031  
MIPS Technologies, Inc.
- [6] MIPS 4K™/5K™ Cache Configuration Application Note  
Document no: MD00213  
MIPS Technologies, Inc.

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## 5 Revision history

| <b>Rev.<br/>Number</b> | <b>Date</b>   | <b>Comments</b>                                                                                                                                       |
|------------------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 01.00                  | Dec. 5, 2001  | First official release.                                                                                                                               |
| 01.01                  | Mar. 4, 2002  | Changed title & structure to support both 4K and 5K FPGA Modules.<br>Removed all LV configuration information and added reference to MD00213 instead. |
| 01.02                  | Mar. 25, 2002 | Added 4KEc, 4KEm, 4KEp and 4KSc RTL version 2.2.0.                                                                                                    |